10/507475

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.(Original): A phase-change memory device comprising:

a substrate;

a plurality of first parallel wiring lines formed above said substrate;

a plurality of second parallel wiring lines formed above said substrate to cross the first wiring lines while being electrically insulated therefrom; and

a plurality of memory cells disposed at respective crossing points of said first wiring lines and said second wiring lines, each said memory cell having one end connected to said first wiring line and the other end connected to said second wiring line, wherein

said memory cell comprises:

a variable resistive element for storing as information a resistance value determined due to phase change between crystalline and amorphous states thereof; and

a Schottky diode connected in series to said variable resistive element.

2. (Original): The phase-change memory device according to claim 1, wherein

said Schottky diode is series-connected to said variable resistive element while having its polarity with said first wiring line side as an anode and with said second wiring line side as a cathode;

said first wiring lines and second wiring lines are potentially fixed in a way such that said Schottky diode of each said memory cell becomes reverse-biased when nonselected; and

said first wiring lines and second wiring lines are selectively pulse-driven during data reading or writing to cause said Schottky diode of said memory cell selected by these lines to become forward-biased.

3. (Original): A phase-change memory device comprising:

a semiconductor substrate;

a plurality of semiconductor layers formed in said semiconductor substrate so that these are arrayed in a matrix form while being partitioned by an element isolation dielectric film;

diodes each formed at its corresponding semiconductor layer with a metal electrode as a terminal electrode, the metal electrode being formed at part of a surface of each said semiconductor layer;

a plurality of first wiring lines provided to commonly connect said diodes as arrayed in one direction of the matrix;

an interlayer dielectric film covering said first wiring lines;

metal plugs buried in space portions of said first wiring lines of said interlayer dielectric film and being in ohmic contact with each said semiconductor layer;

a chalcogenide layer being formed above said interlayer dielectric film and having its bottom surface in contact with said metal plugs; and

a plurality of second wiring lines provided to cross said first wiring lines while being in contact with an upper surface of said chalcogenide layer.

4. (Original): The phase-change memory device according to claim 3, wherein each said diode is a Schottky diode with said metal electrode as an anode electrode.

5. (Original): The phase-change memory device according to claim 3, wherein said semiconductor layers are disposed at a pitch of 2F in the direction of said first wiring lines and also disposed at a pitch of 3F in the direction of said second wiring lines, where F is a minimal device-feature size; and

said first wiring lines and said metal plugs are alternately formed at a pitch of 3F in said second wiring line direction in such a way as to be connected to both end portions of each said semiconductor layer in said second wiring line direction.

6. (Original): A phase-change memory device comprising:

an insulative substrate;

a plurality of first wiring lines formed in parallel with each other above said insulative substrate;

memory cells being formed over each said first wiring line so that one end is connected to each said first wiring line, each said memory cell having a stacked structure of a variable resistive element and a diode, said variable resistive element storing as information a resistance value determined due to phase change between crystalline and amorphous states thereof; and

a plurality of second wiring lines formed over said memory cells to commonly connect together the other end portions of said memory cells arrayed in a direction crossing said first wiring lines.

7. (Original): The phase-change memory device according to claim 6, wherein each said memory cell comprises:

a diode buried in an interlayer dielectric film formed above said first wiring lines so that an upper terminal surface becomes substantially the same in plane position as said interlayer dielectric film while letting a lower terminal surface be connected to a corresponding one of said first wiring lines; and

a chalcogenide layer formed above said interlayer dielectric film with said diode buried therein so that its bottom surface is connected to said upper terminal surface of said diode, said chalcogenide layer becoming said variable resistive element.

8. (Original): The phase-change memory device according to claim 6, wherein said diode is a Schottky diode with said first wiring line side as an anode terminal.

9. (Original): A phase-change memory device comprising:

an insulative substrate; and

a plurality of memory cell arrays stacked over said insulative substrate, wherein

each said memory cell array comprises:

a plurality of first wiring lines extending in parallel with each other;

a plurality of memory cells being formed above each said first wiring line in such a manner that one end is connected to each said first wiring line and each comprising a stacked structure of a variable resistive element and a diode, said variable resistive element storing as information a resistance value determined due to phase change between crystalline and amorphous states thereof; and

a plurality of second wiring lines formed above said memory cells to commonly connect the other ends of said memory cells arrayed in a direction crossing said first wiring lines.

10. (Original): The phase-change memory device according to claim 9, wherein

at least one of said first wiring lines and second wiring lines is shared by two cell arrays adjacent in an up-down direction.

11. (Original): The phase-change memory device according to claim 9, wherein

a layer stack order of said variable resistive element and diode is identical between adjacent cell arrays in an up-down direction.

12. (Original): The phase-change memory device according to claim 9, wherein

a layer stack order of said variable resistive element and diode is inverse between adjacent cell arrays in an up-down direction.

13.(Currently Amended): The phase-change memory device according to claim 6 ~~or 9~~, wherein

said first and second wiring lines are formed with a line/space of 1F/1F, where F is a minimum feature size; and

said memory cells are buried in respective crossing points of said first and second wiring lines.

14. (Original): The phase-change memory device according to claim 9, wherein

said diode of each said memory cell is a Schottky diode being series-connected to said variable resistive element and while having its polarity with said first wiring line side as an anode and with said second wiring line side as a cathode;

said first wiring lines and said second wiring lines are potentially fixed in such a way that said diode of each said memory cell becomes reverse-biased when nonselected; and

during data read or write, said first wiring lines and second wiring lines are selectively pulse-driven to cause said diode of said memory cell selected by these lines to become forward-biased.

15. (Currently Amended): The phase-change memory according to any one of claims 1, ~~3, 6 and 9,~~ further comprising:

selector circuits for fixing said first wiring lines to a state lower in potential than said second wiring lines when nonselected and for selectively supplying

positive and negative logic pulses to said first and second wiring lines respectively during data reading or writing.

16. (Original): The phase-change memory device according to claim 15, wherein

each said selector circuit comprises:

a first select transistor for transferring said positive logic pulse to said first wiring line;

a second select transistor for transferring said negative logic pulse to said second wiring line;

a first reset-use transistor for holding said first wiring line at a first potential level when nonselected; and

a second reset-use transistor for holding said second wiring line at a second potential level higher than the first potential level when nonselected.

17. (Original): The phase-change memory device according to claim 15, further comprising a sense amplifier circuit for comparing a current of said memory cell selected by said selector circuits to a reference value to thereby detect data.

18. (Original): The phase-change memory device according to claim 17, wherein

said sense amplifier circuit comprises at least one of:

a first current detection circuit for comparing to a reference value a current flowing in said first wiring line when said positive and negative logic pulses are given to said first and second wiring lines respectively and for performing level determination; and

a second current detection circuit for comparing to a reference value a current flowing in said second wiring line when said positive and negative logic

pulses are given to said first and second wiring lines respectively and for performing level determination.

19. (Original): The phase-change memory device according to claim 17, wherein

said sense amplifier circuit comprises:

a dummy cell having its resistance value midway between a high resistance state and a low resistance state of said memory cells;

a first resistor interposed between said first wiring line and a first power supply line to which said positive logic pulse is given;

a second resistor interposed between said second wiring line and a second power supply line to which said negative logic pulse is given;

a third resistor interposed between one end of said dummy cell and said first power supply line;

a fourth resistor interposed between the other end of said dummy cell and said second power supply line;

a first operational amplifier for comparison between an intermediate tap output voltage of said first resistor and a voltage at a connection node of said third resistor and said dummy cell; and

a second operational amplifier for comparison between an intermediate tap output voltage of said second resistor and a voltage at a connection node of said fourth resistor and said dummy cell.

20. (Original): The phase-change memory device according to claim 9, wherein

write and read of multiple-value information are performed by combination of a high resistance state and a low resistance state of the respective memory cells accessed simultaneously in said plurality of cell arrays.

21. (Original): The phase-change memory device according to claim 20, wherein

said plurality of cell arrays has a first cell array and a second cell array stacked over said first cell array, said first and second cell arrays sharing said first wiring lines; and

write and read of four-value information are performed by combination of said high resistance state and said low resistance state of two memory cells accessed simultaneously in said first and second cell arrays.

22. (Original): The phase-change memory device according to claim 21, further comprising a sense amplifier circuit for detection of said four-value information, wherein

said sense amplifier circuit comprises:

a first current detection circuit for comparing a current flowing in said second wiring line of said first cell array to a reference value and for performing level determination;

a second current detection circuit for comparing a current flowing in said first wiring line shared by said first and second cell arrays to a reference value and for performing level determination; and

a third current detection circuit for comparing a current flowing in said second wiring line of said second cell array to a reference value and for performing level determination.

23. (Original): The phase-change memory device according to claim 20, wherein

said plurality of cell arrays has a first cell array, a second cell array stacked over said first cell array, said first and second cell arrays sharing said first wiring lines, and a third cell array stacked over said second cell array, said second and third cell arrays sharing said second wiring lines; and

write and read of eight-value information are performed by combination of said high resistance state and said low resistance state of three memory cells accessed simultaneously in said first to three cell arrays.

24. (Original): The phase-change memory device according to claim 23, further comprising a sense amplifier circuit for detection of said eight-value information, wherein

said sense amplifier circuit comprises:

a first current detection circuit for comparing a current flowing in said second wiring line of said first cell array to a reference value and for performing level determination;

a second current detection circuit for comparing a current flowing in said first wiring line shared by said first and second cell arrays to a reference value and for performing level determination;

a third current detection circuit for comparing a current flowing in said second wiring line shared by said second and third cell arrays to a reference value and for performing level determination; and

a fourth current detection circuit for comparing a current flowing in said first wiring line of said third cell array to a reference value and for performing level determination.

25. (Original): The phase-change memory device according to claim 24, wherein

said second current detection circuit comprises two current detection units for determining a difference in current value between a case of two selected memory cells of said first and second cell arrays being both in said low resistance state and a case of either one being in said low resistance state.

26. (Original): The phase-change memory device according to claim 24, wherein

said third current detection circuit comprises two current detection units for determining a difference in current value between a case of two selected memory cells of said second and third cell arrays being both in said low resistance state and a case of either one being in said low resistance state.

27. (Original): The phase-change memory device according to claim 15, further comprising a write circuit for supplying a positive logic pulse and a negative logic pulse to said first wiring line and said second wiring line respectively with respect to a memory cell as selected by said selection circuit, for writing said low resistance state due to complete overlap of pulse widths of said positive logic pulse and negative logic pulse, and for wiring said high resistance state due to partial overlap of pulse widths of said positive logic pulse and negative logic pulse.

28. (Original): The phase-change memory device according to claim 27, wherein

said write circuit has a pulse voltage booster circuit for selectively boosting either one of said positive logic pulse and said negative logic pulse at an overlap portion of pulse widths of said positive logic pulse and negative logic pulse when writing said high resistance state.

29. (Original): The phase-change memory device according to claim 20, further comprising a write circuit for writing, based on write pulse width control, multi-value information into a plurality of simultaneously accessed memory cells of said plurality of cell arrays, said multi-value information being represented by combination of said high resistance state and said low resistance state within said plurality of simultaneously accessed memory cells.

30. (Original): The phase-change memory device according to claim 29, wherein

said write circuit comprises:

a pulse generation circuit for generating two types of pulses different in pulse width from each other; and

a logic gate circuit for determining in accordance with said multi-value information the time width of a write pulse being given between the simultaneously selected first and second wiring lines of a cell array by selection and combination of two types of pulses as output from said pulse generation circuit.

31. (Original): The phase-change memory device according to claim 29, wherein

said write circuit comprises:

a pulse generation circuit for generating two types of pulses with a constant pulse width and with a time difference therebetween; and

a logic gate circuit for determining in accordance with said multi-value information the time width of an overlap of said positive logic pulse and said negative logic pulse being given to the simultaneously selected first and second wiring lines of a cell array respectively by selection and combination of said two types of pulses as output from said pulse generation circuit.

32. (Currently Amended): The phase-change memory device according to claim 30 ~~or 31~~, wherein

said write circuit comprises a pulse voltage booster circuit for selectively boosting said positive logic pulse or said negative logic pulse being output from said logic gate circuit in accordance with said multi-value information to be written.

33. (Original): The phase-change memory device according to claim 9, wherein

in said plurality of cell arrays, a plurality of cell blocks are defined as three-dimensional cell assemblies, each cell blocks being surrounded by first virtual boundaries with a predetermined interval being in parallel to said first wiring lines and perpendicular to a cell array plane and second virtual boundaries with a prespecified interval being in parallel to said second wiring lines and perpendicular to said cell array plane; and

data access is performed in units of said cell blocks.